CLAIMS

WHAT IS CLAIMED IS:

1. An oversampling FIR filter for filtering with a clock having a frequency higher than a frequency of accepting input data, comprising:

a shift register having a plurality of holding parts connected in cascade for sequentially accepting input data;

a plurality of selectors respectively formed corresponding to said holding parts for selecting, from a plurality of tap factors, a predetermined number of tap factors in synchronization with said clock;

a plurality of multipliers formed respectively corresponding to said holding parts for respectively multiplying said input data held in said holding parts, by said tap factors selected by said selectors corresponding to said holding parts; and

an adder for adding the multiplication results from said multipliers and outputting the resultants as output data, and wherein

said selectors change said predetermined number of tap factors to be selected, in accordance with a change in the number of oversamples, which is the number of tap factors to be multiplied by said single input data.

2. The oversampling FIR filter according to claim 1, wherein a part of said plurality of tap factors respectively selectable by said selectors adjacent to one another are shared by said selectors.

3. The oversampling FIR filter according to claim 2, comprising a tap controlling unit for instructing said selectors said tap factor to be selected first in accordance with a change in said number of oversamples.

4. The oversampling FIR filter according to claim 2, wherein when said number of oversamples is changed, said tap controlling unit changes said tap factors selected by said

selectors back to said predetermined tap factors used prior to the changing of said number of oversamples, in which every time said input data is accepted, the changes of said tap factors are performed in sequence, starting from said selector corresponding to said holding part at the input side.

5. A method for controlling an oversampling FIR filter for filtering with a clock having a frequency higher than a frequency of accepting input data, comprising the steps of:

sequentially accepting input data at a shift register having a plurality of holding parts connected in cascade;

sequentially selecting, from a plurality of tap factors, a predetermined number of tap factors in synchronization with said clock by a plurality of selectors respectively formed corresponding to said holding parts;

respectively multiplying said input data held in said holding parts by said tap factors selected by said selectors corresponding to said holding parts; and

adding the multiplication results and outputting the resultants as output data; and

changing said predetermined number of tap factors to be selected by said selectors, in accordance with a change in the number of oversamples, which is the number of tap factors to be multiplied by said single input data.

6. The method for controlling an oversampling FIR filter according to claim 5, wherein a part of said plurality of tap factors respectively selectable by said selectors adjacent to one another are shared by said selectors.

7. The method for controlling an oversampling FIR filter according to claim 6, comprising the step of instructing said selectors said tap factor to be selected first in accordance with a change in said number of oversamples.

8. The method for controlling an oversampling FIR filter according to claim 6, comprising the step of changing said tap factors selected by said selectors back to said

predetermined tap factors used prior to the changing of said number of oversamples when said number of oversamples is changed, in which every time said input data is accepted, said changes of said tap factors are performed in sequence, starting from said selector corresponding to said holding part at the input side.

9. A semiconductor integrated circuit having an oversampling FIR filter, wherein said oversampling filter comprises:

a shift register having a plurality of holding parts connected in cascade for sequentially accepting input data;

a plurality of selectors respectively formed corresponding to said holding parts for selecting predetermined number of tap factors in synchronization with said clock from a plurality of tap factors;

a plurality of multipliers formed respectively corresponding to said holding parts for respectively multiplying said input data held in said holding parts by said tap factors selected by said selectors corresponding to said holding parts; and

an adder for adding the multiplication results from said multipliers and outputting the resultants as output data, and wherein

said selectors change said predetermined number of tap factors to be selected, in accordance with a change in the number of oversamples, which is the number of tap factors to be multiplied by said single input data.

10. A communication system wherein data filtered with an oversampling FIR filter is transmitted, wherein said oversampling FIR filter comprises:

a shift register having a plurality of holding parts connected in cascade for sequentially accepting input data;

a plurality of selectors respectively formed corresponding to said holding parts for selecting predetermined number of tap factors in synchronization with said clock from a

plurality of tap factors;

a plurality of multipliers formed respectively corresponding to said holding parts for respectively multiplying said input data held in said holding parts by said tap factors selected by said selectors corresponding to said holding parts; and

an adder for adding the multiplication results from said multipliers and outputting the resultants as output data, and wherein

said selectors change said predetermined number of tap factors to be selected, in accordance with a change in the number of oversamples, which is the number of tap factors to be multiplied by said single input data.